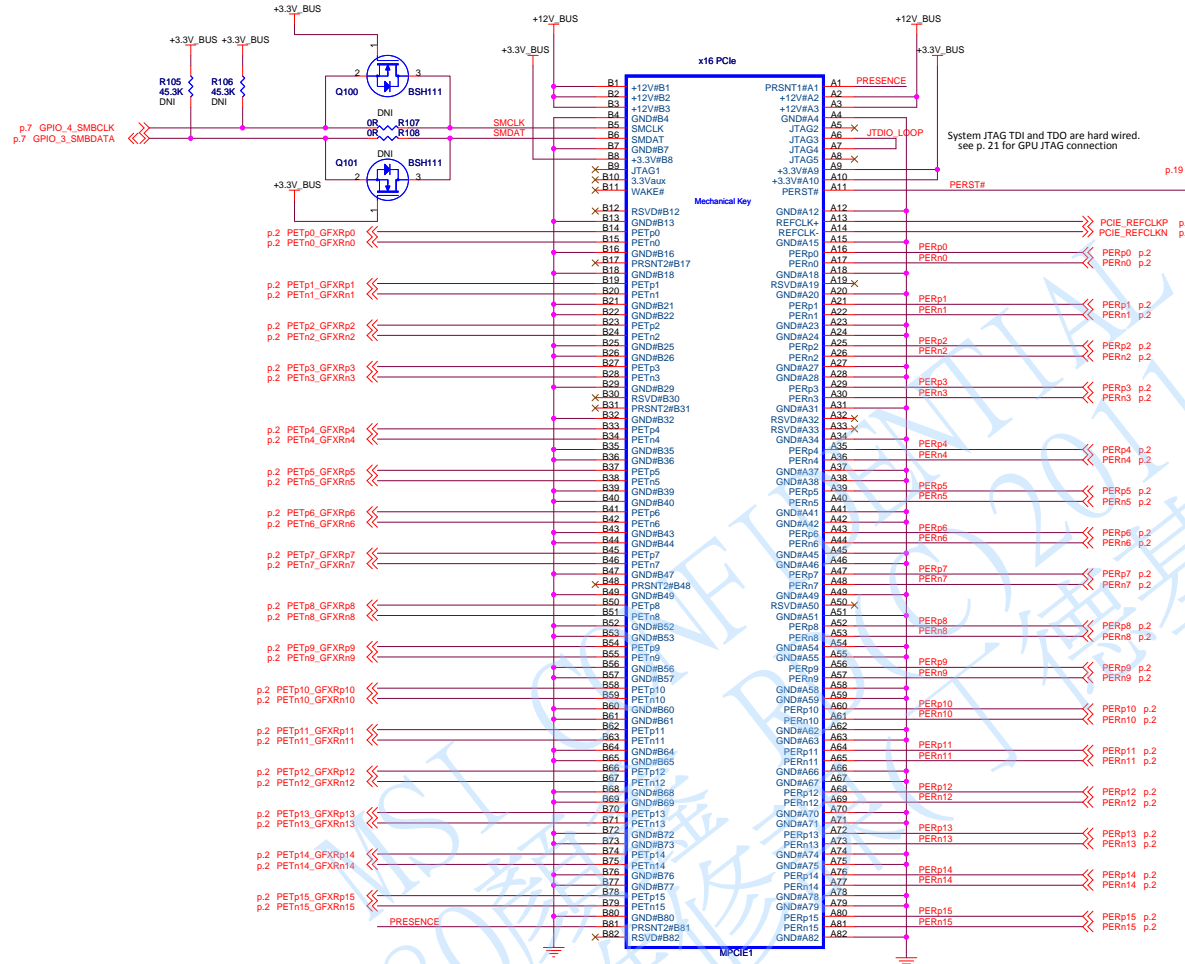
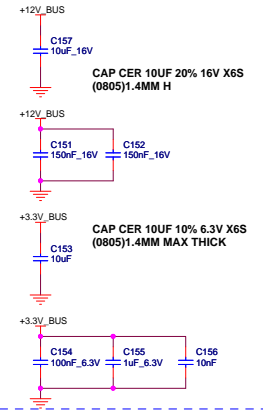


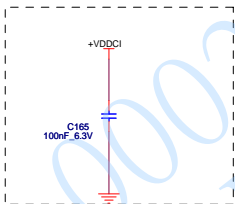
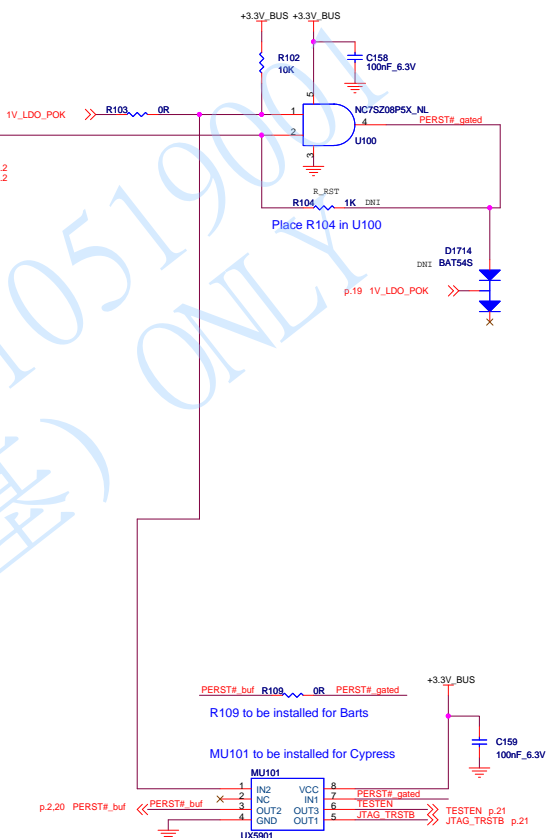
PCI-EXPRESS EDGE CONNECTOR



Place these caps as close to the PCIe connector as possible



PCIe RESET Buffered



SYMBOL LEGEND	
DNI	DO NOT INSTALL
#	ACTIVE LOW
	DIGITAL GROUND
	ANALOG GROUND
	BRING UP ONLY

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Date: Thursday, June 10, 2010
Sheet 1 of 23

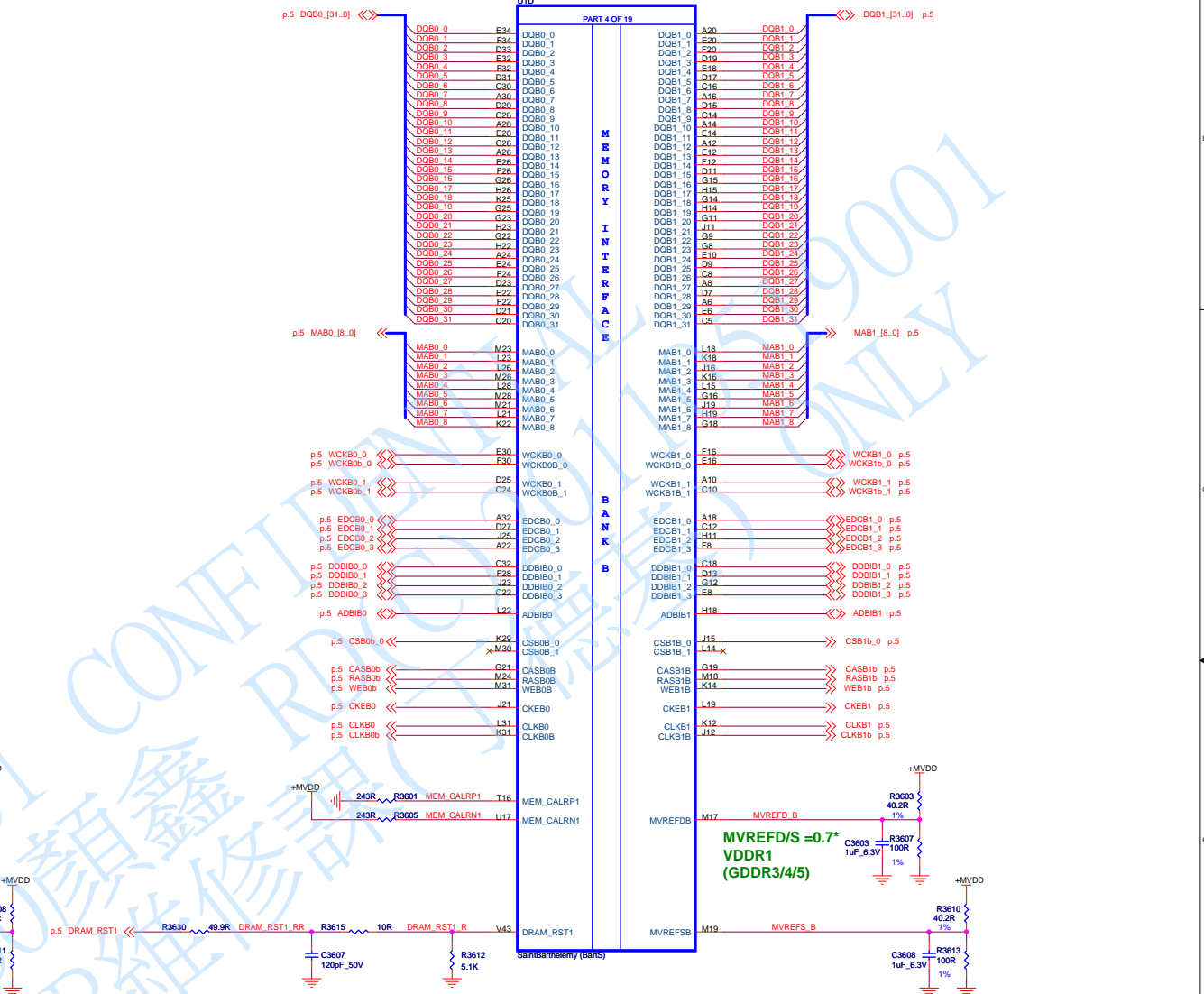
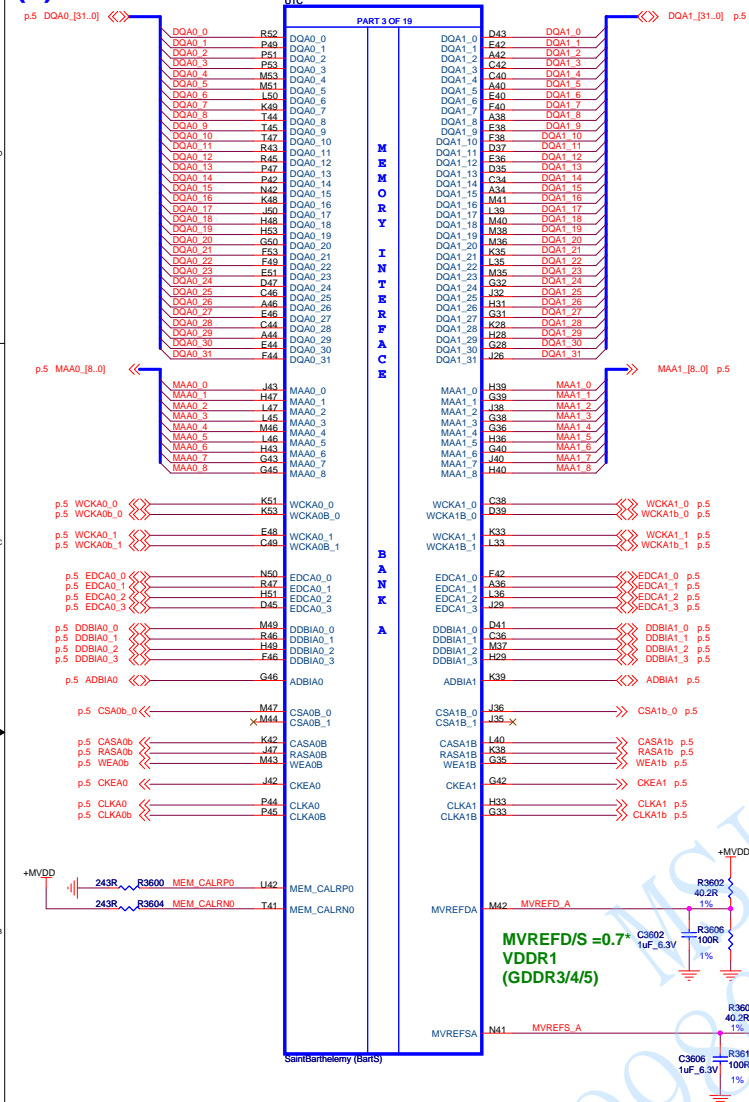
Rev 1

Doc No. 105-C224XX-00A

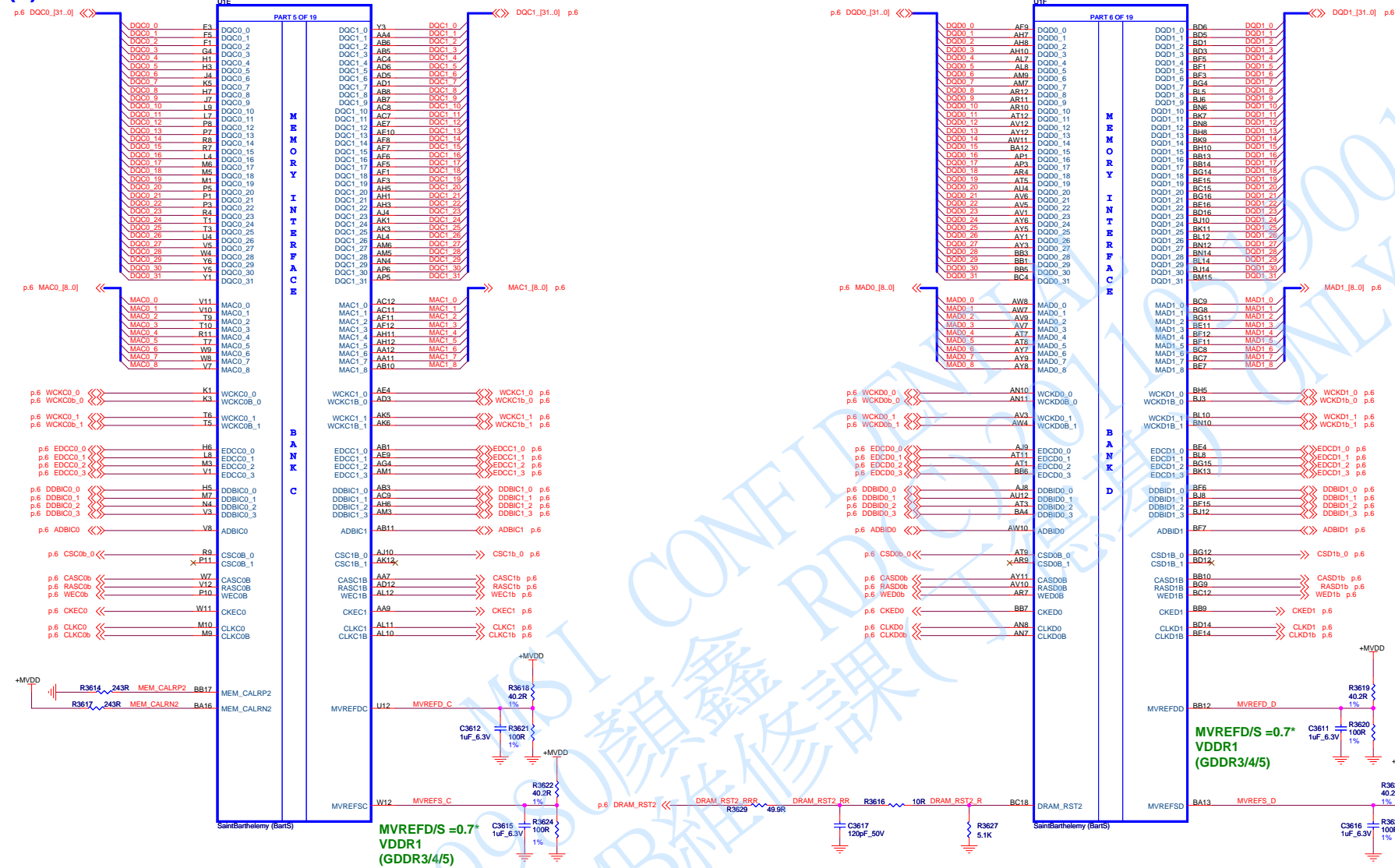
Title PCIe EDGE CONNECTOR

Doc No. 105 G224XX 00A

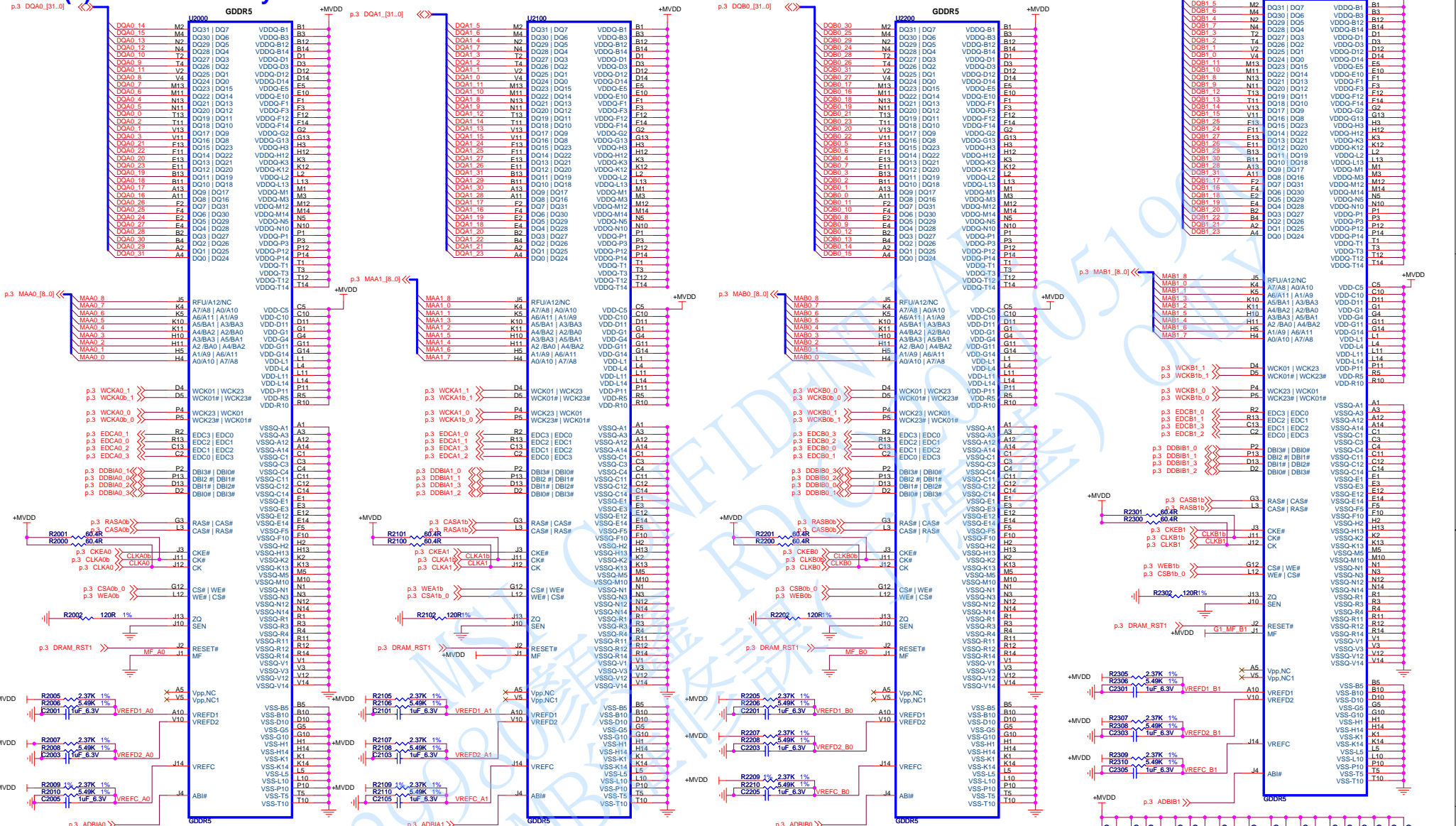
(3) Barts MEM Interface Ch A&B



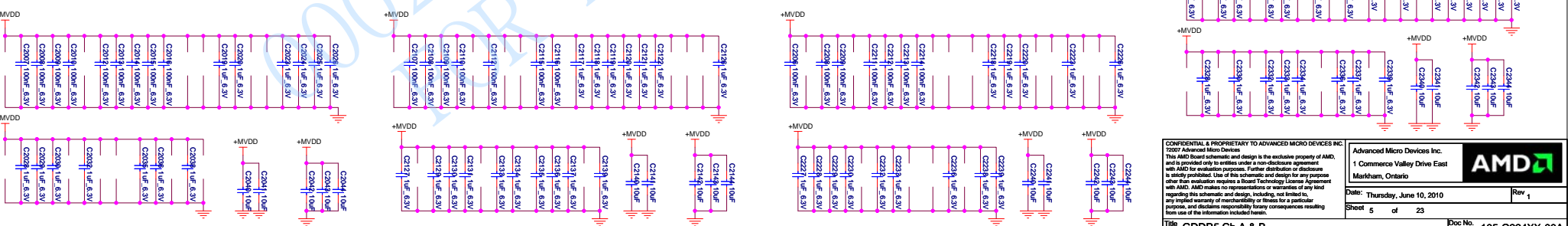
(4) Barts MEM Interface Ch C&D



(5) GDDR5 Memory Channel A&B

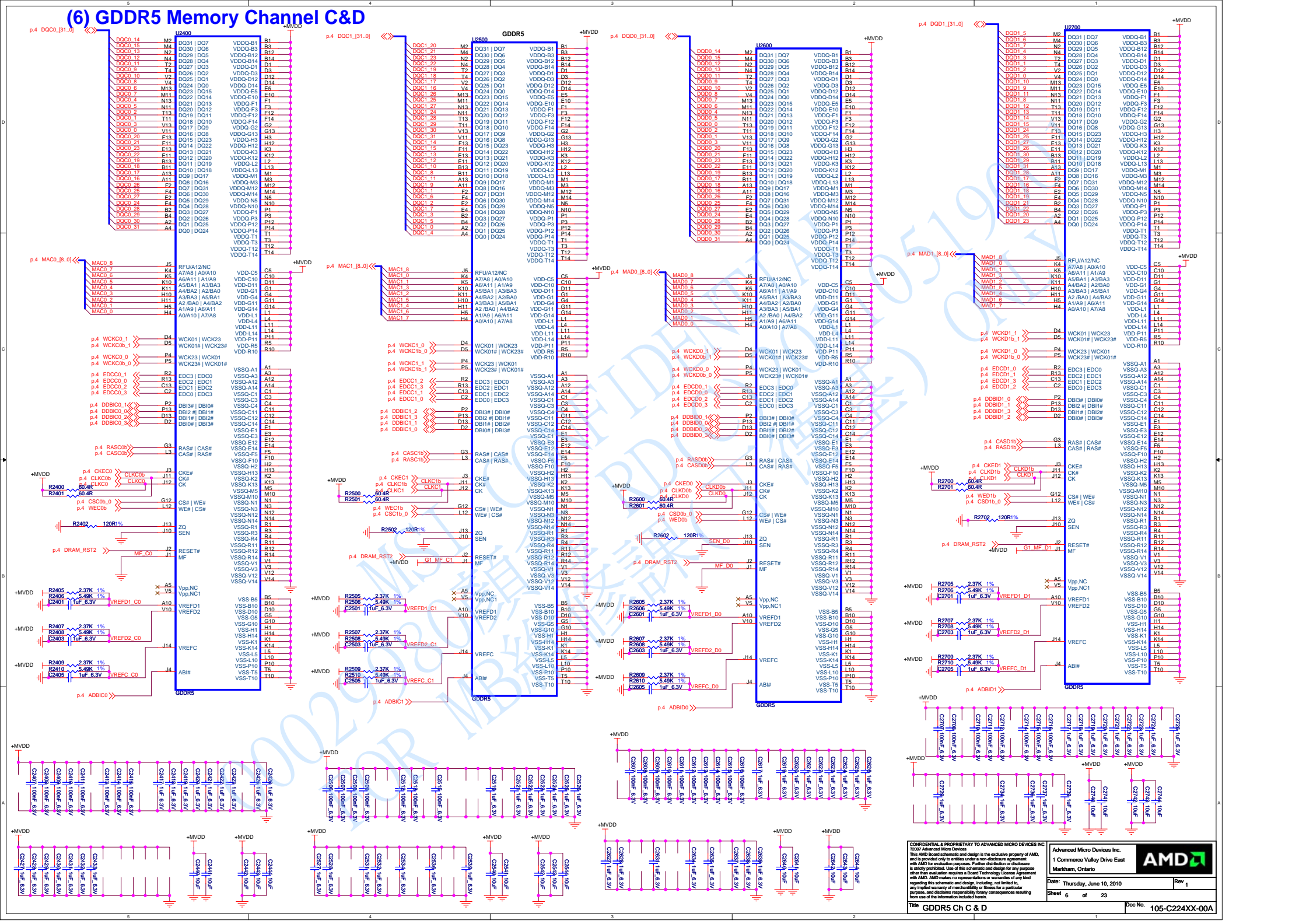


Use internal Vref memory voltage

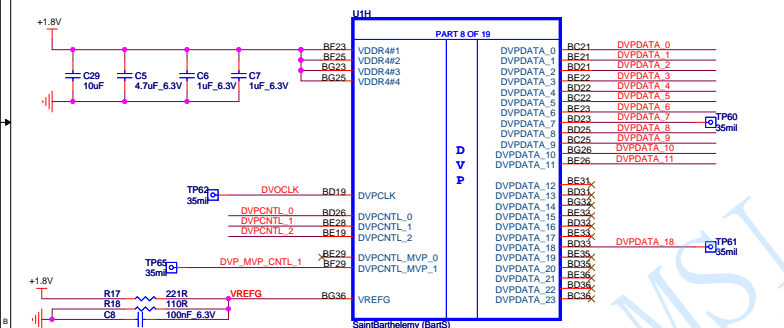
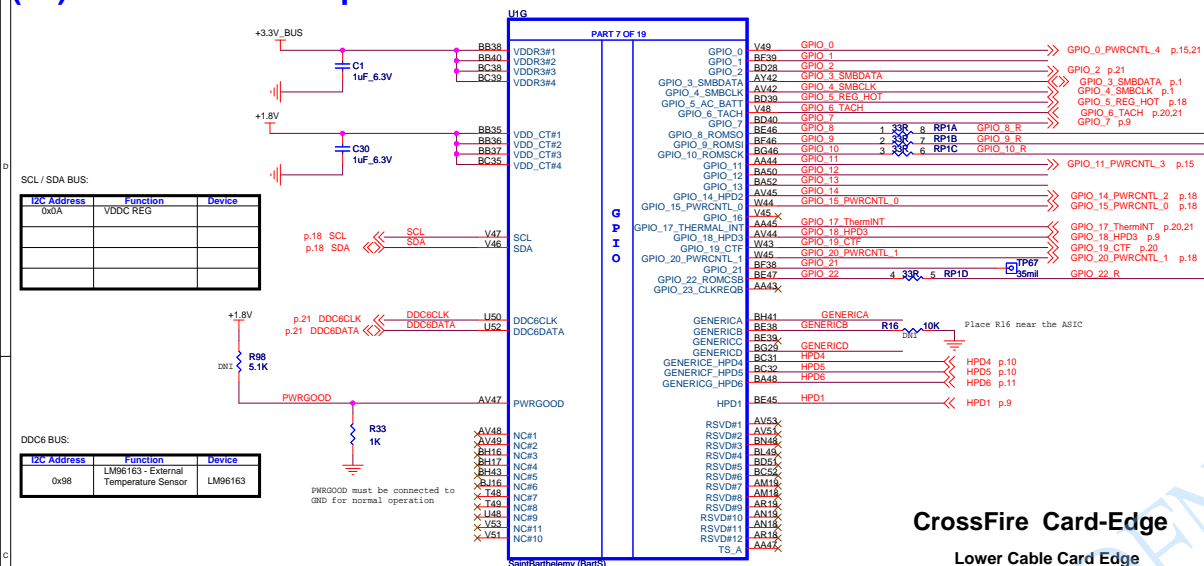



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Sheet	5 of 23
Title	Doc No. 105-C224XX-00A


(6) GDDR5 Memory Channel C&D

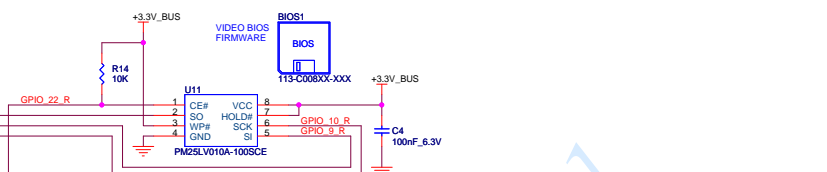
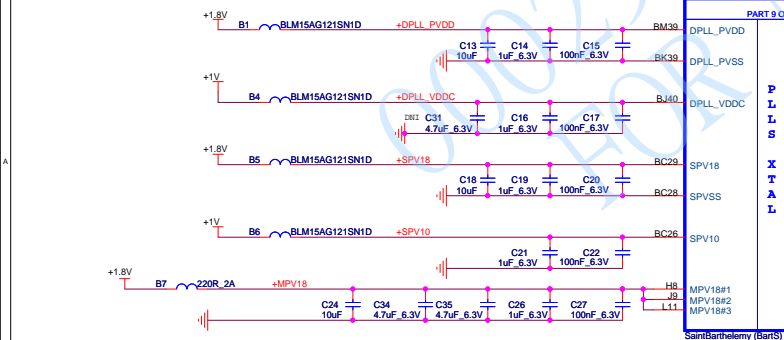


(07) Barts GPIOs Strap CF XTAL OSC

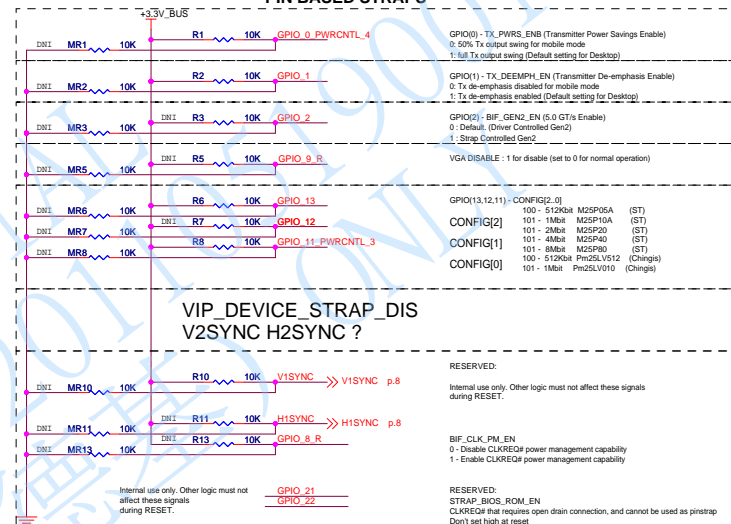


 Place the crossfire testpoints near the ASIC and not the connector

 Please pay attention to the grounding strategies for these filter capacitors to maintain a close loop for current.

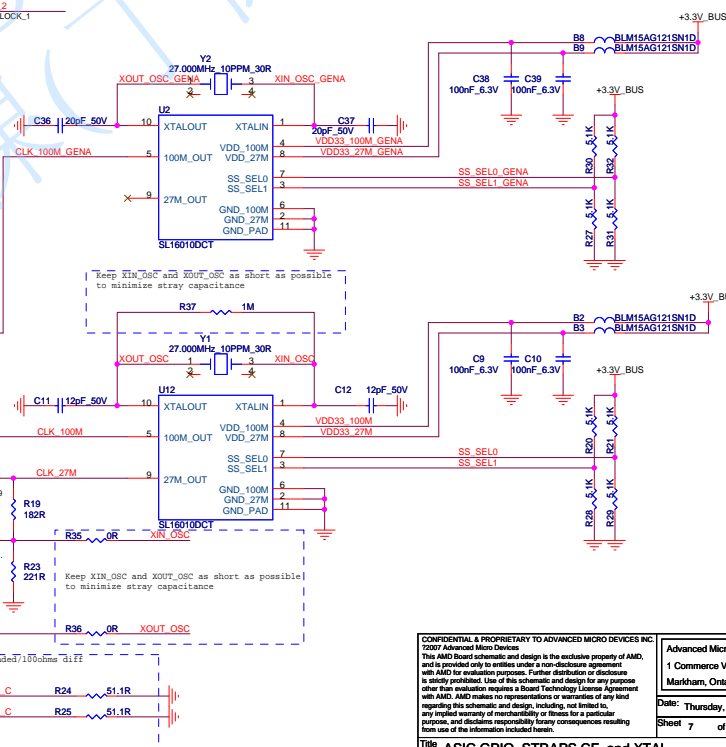
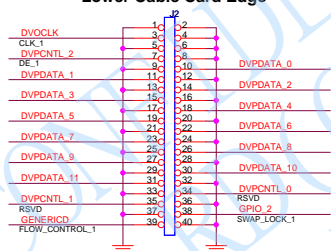


PIN BASED STRAPS



CrossFire Card-Edge

Lower Cable Card Edge



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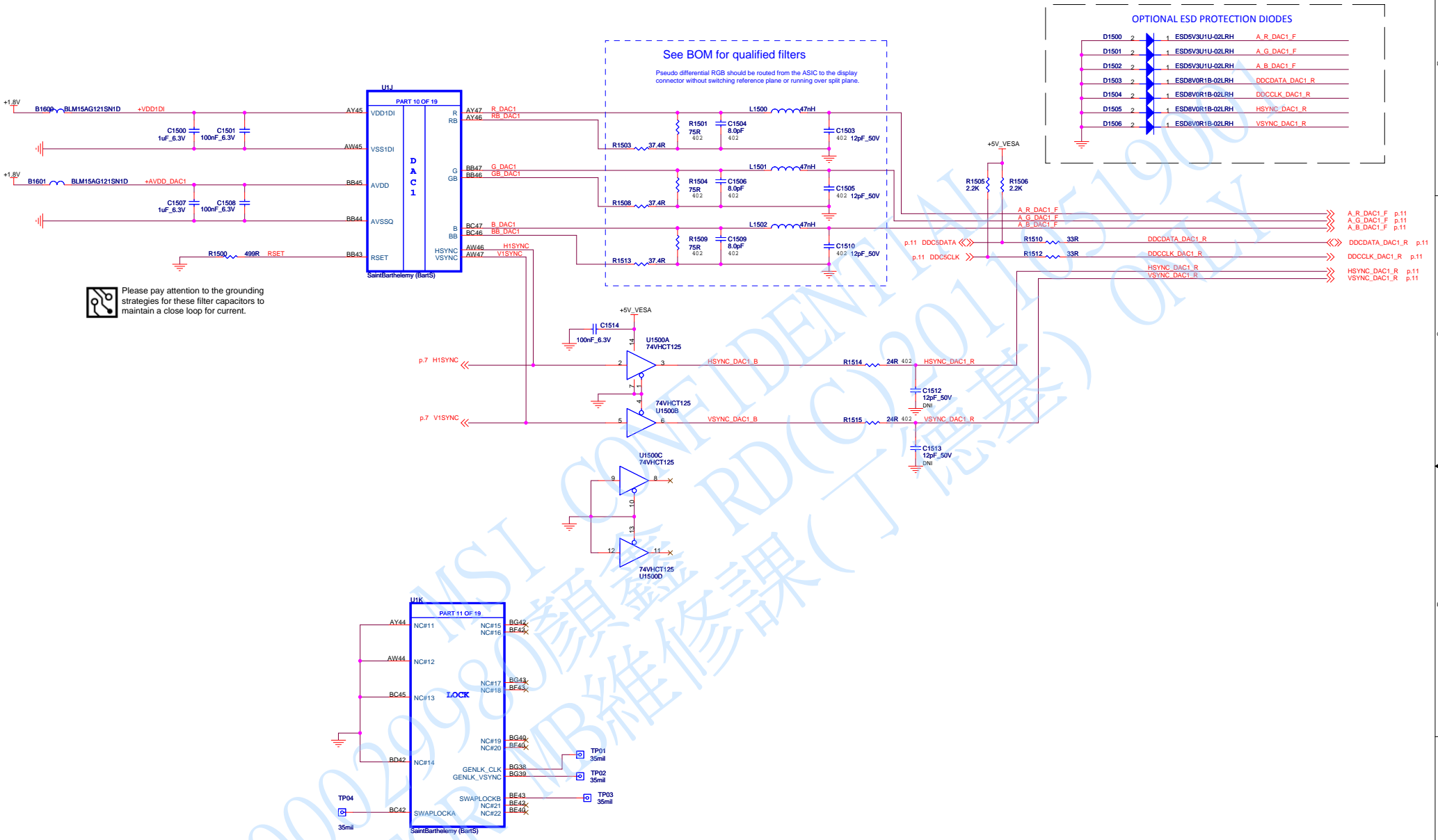
Sheet 7 of 23

Rev

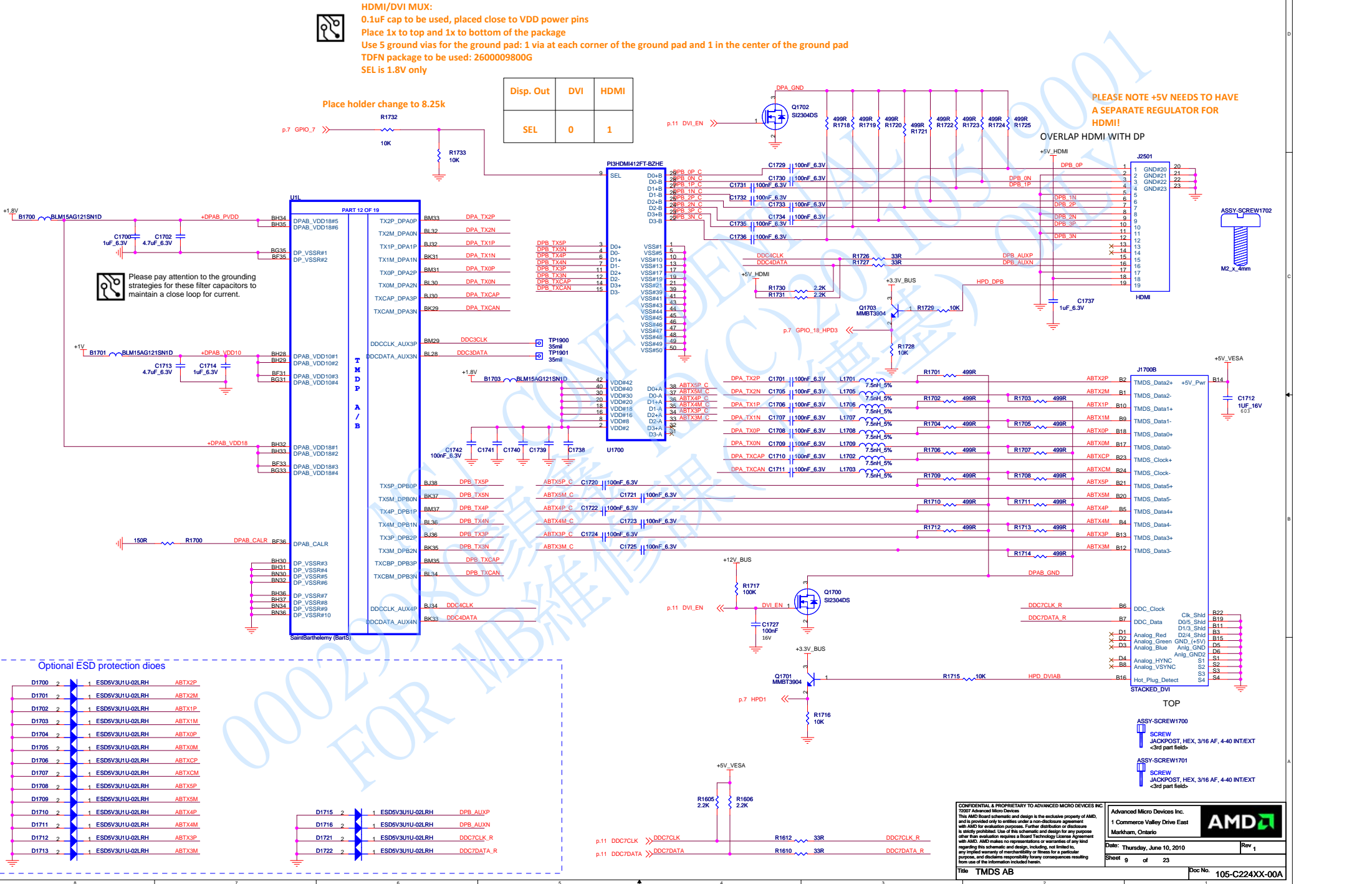
Title ASIC GPIO, STRAPS, CF, and XTAL

Doc No. 105-C224XX-00A

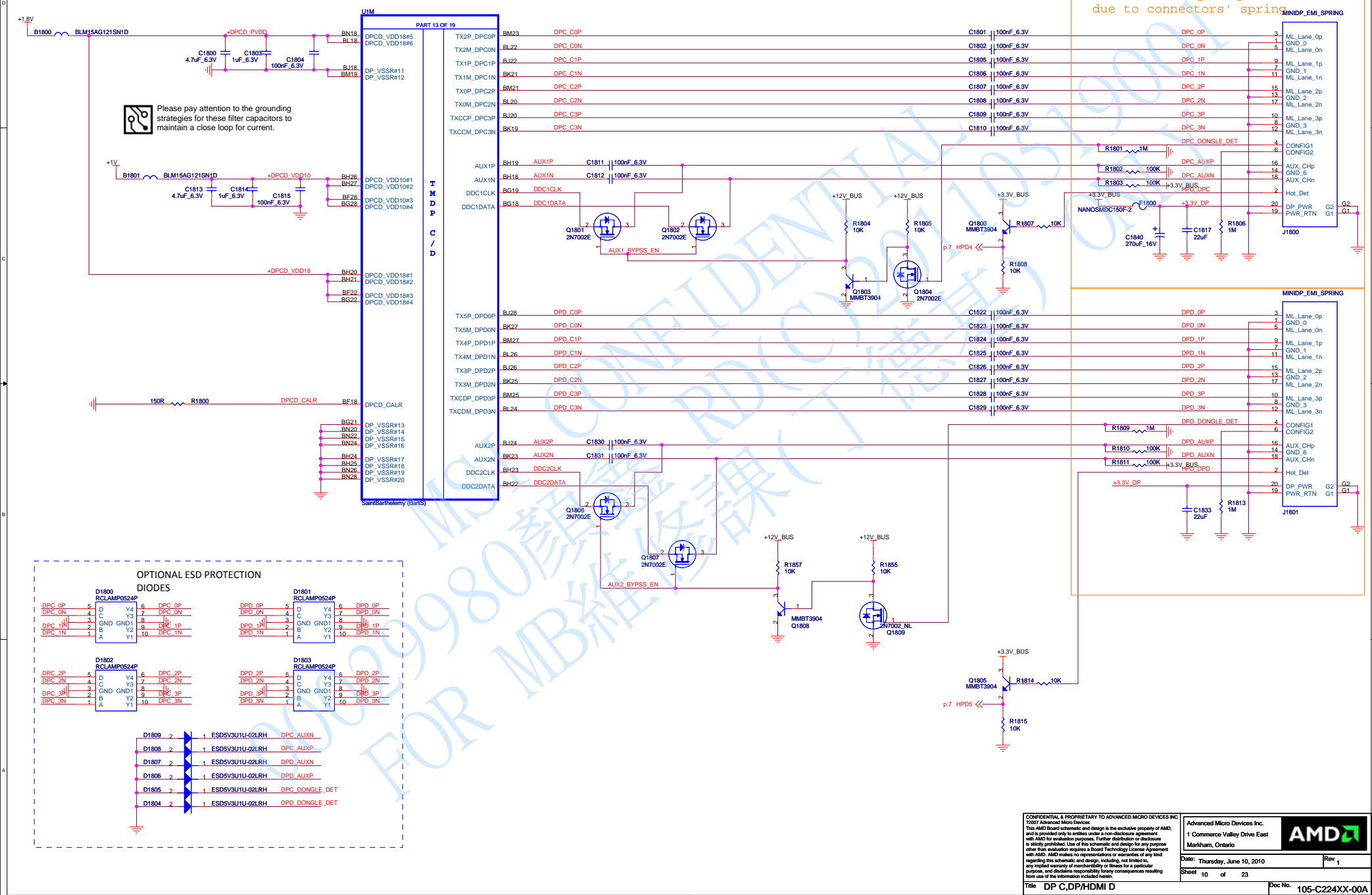
(08) Barts DAC1



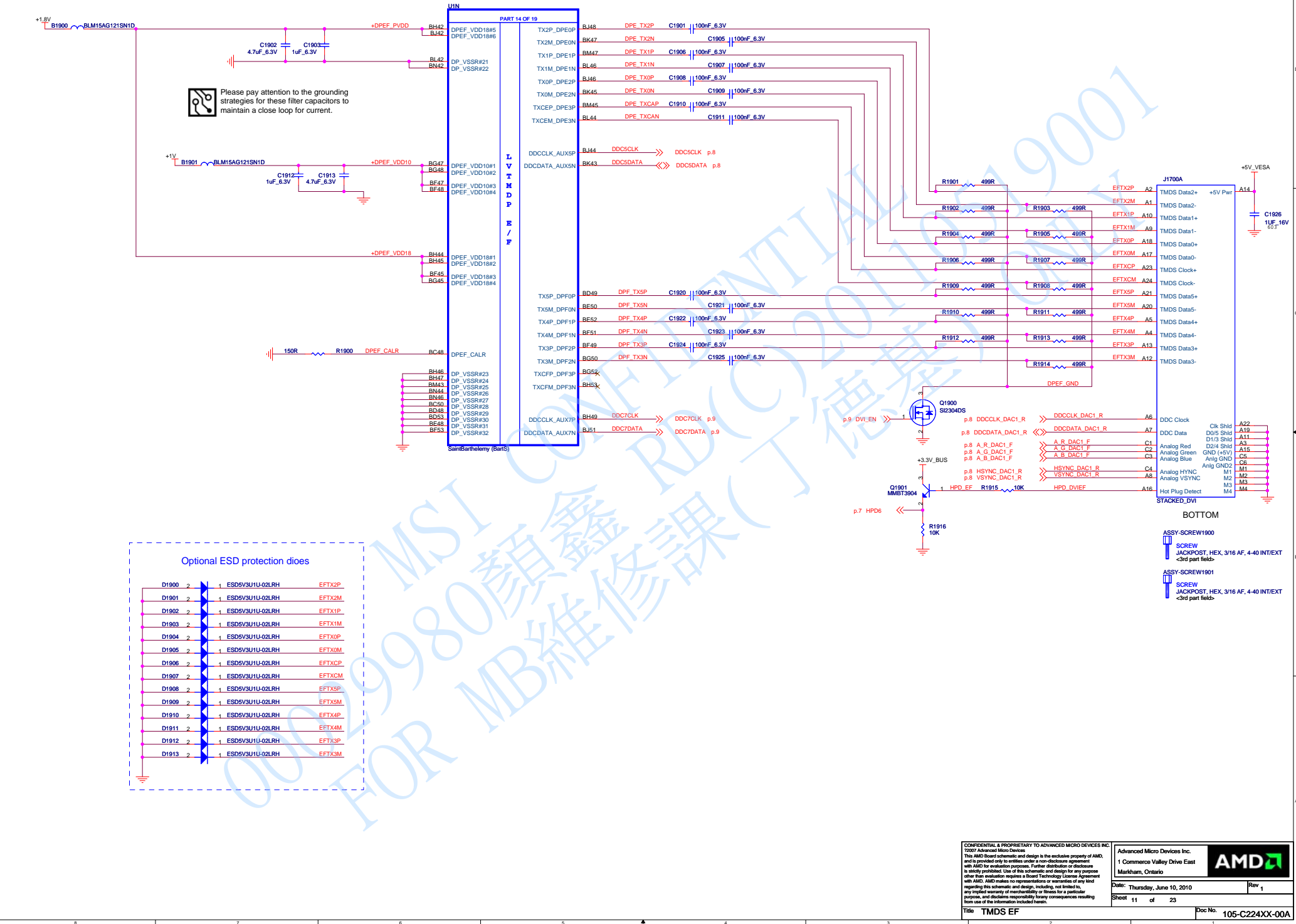
(09) Barts TMD5 A&B



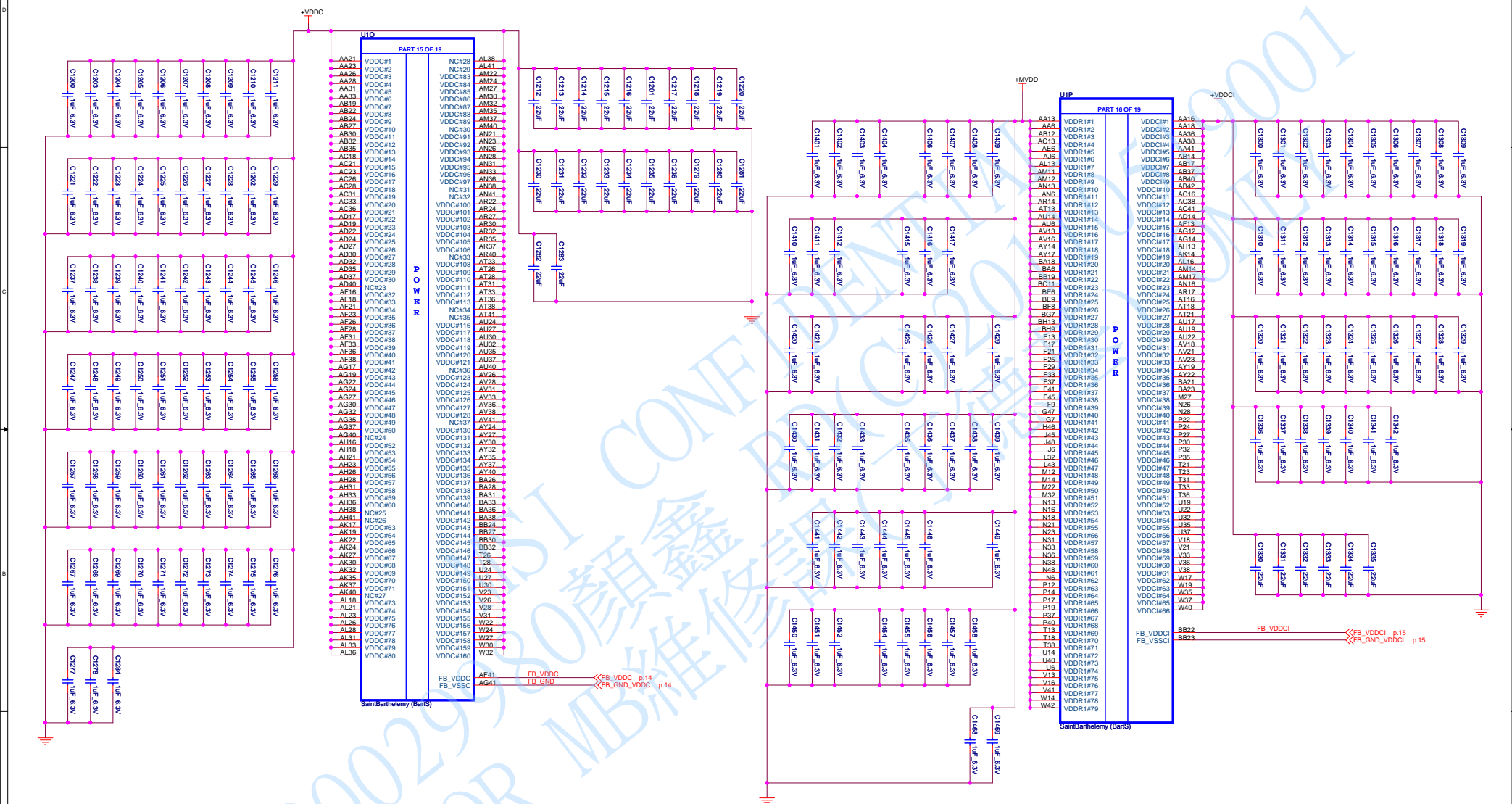
(10) Barts Display Port/HDMI C&D



(11) Barts LVTMDP E&F



(12) Barts Power



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Date: Thursday, June 10, 2010
Sheet 12 of 23

Rev

Doc No. 105-C324XY-00A

(13) Barts GND

UIC			UIR		
PART 17 OF 19			PART 18 OF 19		
A46	VSS#1	VSS#126	BA17	VSS#251	VSS#376
AA10	VSS#2	VSS#127	BA19	VSS#252	VSS#377
AA14	VSS#3	VSS#128	BA2	VSS#253	VSS#378
AA17	VSS#4	VSS#129	BA22	VSS#254	VSS#379
AA19	VSS#5	VSS#130	BA24	VSS#255	VSS#380
AA2	VSS#6	VSS#131	BA27	VSS#256	VSS#381
AA22	VSS#7	VSS#132	BA30	VSS#257	VSS#382
AA24	VSS#8	VSS#133	BA32	VSS#258	VSS#383
AA27	VSS#9	VSS#134	BA33	VSS#259	VSS#384
AA30	VSS#10	VSS#135	BA37	VSS#260	VSS#385
AA32	VSS#11	VSS#136	BA40	VSS#261	VSS#386
AA35	VSS#12	VSS#137	BA41	VSS#262	VSS#387
AA37	VSS#13	VSS#138	BA11	VSS#263	VSS#388
AA40	VSS#14	VSS#139	BA16	VSS#264	VSS#389
AA42	VSS#15	VSS#140	BA18	VSS#265	VSS#390
AA5	VSS#16	VSS#141	BA21	VSS#266	VSS#391
AB13	VSS#17	VSS#142	BA23	VSS#267	VSS#392
AB16	VSS#18	VSS#143	BA28	VSS#268	VSS#393
AB18	VSS#19	VSS#144	BA31	VSS#269	VSS#394
AB1	VSS#20	VSS#145	BA33	VSS#270	VSS#395
AB23	VSS#21	VSS#146	BA40	VSS#271	VSS#396
AB28	VSS#22	VSS#147	BB51	VSS#272	VSS#397
AB33	VSS#23	VSS#148	VSS#273	VSS#398	VSS#398
AB31	VSS#24	VSS#149	VSS#274	VSS#399	VSS#399
AB35	VSS#25	VSS#150	BB9	VSS#275	VSS#400
AB37	VSS#26	VSS#151	BC10	VSS#276	VSS#401
AB38	VSS#27	VSS#152	BC16	VSS#277	VSS#402
AB41	VSS#28	VSS#153	BC2	VSS#278	VSS#403
AC10	VSS#29	VSS#154	BC23	VSS#279	VSS#404
AC17	VSS#30	VSS#155	BC33	VSS#280	VSS#405
AC19	VSS#31	VSS#156	BC40	VSS#281	VSS#406
AC2	VSS#32	VSS#157	BC6	VSS#282	VSS#407
AC22	VSS#33	VSS#158	BD15	VSS#283	VSS#408
AC24	VSS#34	VSS#159	BD18	VSS#284	VSS#409
AC27	VSS#35	VSS#160	BD29	VSS#285	VSS#410
AC30	VSS#36	VSS#161	BD38	VSS#286	VSS#411
AC32	VSS#37	VSS#162	BE12	VSS#287	VSS#412
AC35	VSS#38	VSS#163	BE19	VSS#288	VSS#413
AC37	VSS#39	VSS#164	BE25	VSS#289	VSS#414
AC40	VSS#40	VSS#165	BE3	VSS#290	VSS#415
AC42	VSS#41	VSS#166	BE4	VSS#291	VSS#416
AC6	VSS#42	VSS#167	BE14	VSS#292	VSS#417
AD13	VSS#43	VSS#168	BE16	VSS#293	VSS#418
AD16	VSS#44	VSS#169	BE19	VSS#294	VSS#419
AD21	VSS#45	VSS#170	BE21	VSS#295	VSS#420
AD23	VSS#46	VSS#171	BE26	VSS#296	VSS#421
AD28	VSS#47	VSS#172	BE32	VSS#297	VSS#422
AD31	VSS#48	VSS#173	BE3	VSS#298	VSS#423
AD33	VSS#49	VSS#174	BE9	VSS#299	VSS#424
AD38	VSS#50	VSS#175	BE2	VSS#300	VSS#425
AD41	VSS#51	VSS#176	BE11	VSS#301	VSS#426
AD43	VSS#52	VSS#177	BE12	VSS#302	VSS#427
AD48	VSS#53	VSS#178	BE11	VSS#303	VSS#428
AD51	VSS#54	VSS#179	BE12	VSS#304	VSS#429
AD53	VSS#55	VSS#180	BE14	VSS#305	VSS#430
AD58	VSS#56	VSS#181	BE15	VSS#306	VSS#431
AE2	VSS#57	VSS#182	BE18	VSS#307	VSS#432
AE5	VSS#58	VSS#183	BE39	VSS#308	VSS#433
AE10	VSS#59	VSS#184	BE40	VSS#309	VSS#434
AE14	VSS#60	VSS#185	BE41	VSS#310	VSS#435
AE17	VSS#61	VSS#186	BE45	VSS#311	VSS#436
AE22	VSS#62	VSS#187	BE46	VSS#312	VSS#437
AE24	VSS#63	VSS#188	BE48	VSS#313	VSS#438
AE27	VSS#64	VSS#189	BE49	VSS#314	VSS#439
AE30	VSS#65	VSS#190	BE51	VSS#315	VSS#440
AE32	VSS#66	VSS#191	BE52	VSS#316	VSS#441
AE35	VSS#67	VSS#192	BE53	VSS#317	VSS#442
AE37	VSS#68	VSS#193	BE54	VSS#318	VSS#443
AE40	VSS#69	VSS#194	BE55	VSS#319	VSS#444
AE42	VSS#70	VSS#195	BE56	VSS#320	VSS#445
AE48	VSS#71	VSS#196	BE57	VSS#321	VSS#446
AG13	VSS#72	VSS#197	BE58	VSS#322	VSS#447
AG16	VSS#73	VSS#198	BE59	VSS#323	VSS#448
AG2	VSS#74	VSS#199	BE60	VSS#324	VSS#449
AG21	VSS#75	VSS#200	BE61	VSS#325	VSS#450
AG26	VSS#76	VSS#201	BE62	VSS#326	VSS#451
AG28	VSS#77	VSS#202	BE63	VSS#327	VSS#452
AG31	VSS#78	VSS#203	BE64	VSS#328	VSS#453
AG33	VSS#79	VSS#204	BE65	VSS#329	VSS#454
AG35	VSS#80	VSS#205	BE66	VSS#330	VSS#455
AG38	VSS#81	VSS#206	BE67	VSS#331	VSS#456
AG40	VSS#82	VSS#207	BE68	VSS#332	VSS#457
AG42	VSS#83	VSS#208	BE69	VSS#333	VSS#458
AG48	VSS#84	VSS#209	BE70	VSS#334	VSS#459
AG51	VSS#85	VSS#210	BE71	VSS#335	VSS#460
AG53	VSS#86	VSS#211	BE72	VSS#336	VSS#461
AG58	VSS#87	VSS#212	BE73	VSS#337	VSS#462
AG62	VSS#88	VSS#213	BE74	VSS#338	VSS#463
AG65	VSS#89	VSS#214	BE75	VSS#339	VSS#464
AG68	VSS#90	VSS#215	BE76	VSS#340	VSS#465
AG72	VSS#91	VSS#216	BE77	VSS#341	VSS#466
AG75	VSS#92	VSS#217	BE78	VSS#342	VSS#467
AG78	VSS#93	VSS#218	BE79	VSS#343	VSS#468
AG82	VSS#94	VSS#219	BE80	VSS#344	VSS#469
AG85	VSS#95	VSS#220	BE81	VSS#345	VSS#470
AG88	VSS#96	VSS#221	BE82	VSS#346	VSS#471
AG92	VSS#97	VSS#222	BE83	VSS#347	VSS#472
AG95	VSS#98	VSS#223	BE84	VSS#348	VSS#473
AG98	VSS#99	VSS#224	BE85	VSS#349	VSS#474
AK13	VSS#100	VSS#225	BE86	VSS#350	VSS#475
AK16	VSS#101	VSS#226	BE87	VSS#351	VSS#476
AK18	VSS#102	VSS#227	BE88	VSS#352	VSS#477
AK21	VSS#103	VSS#228	BE89	VSS#353	VSS#478
AK23	VSS#104	VSS#229	BE90	VSS#354	VSS#479
AK26	VSS#105	VSS#230	BE91	VSS#355	VSS#480
AK28	VSS#106	VSS#231	BE92	VSS#356	VSS#481
AK31	VSS#107	VSS#232	BE93	VSS#357	VSS#482
AK33	VSS#108	VSS#233	BE94	VSS#358	VSS#483
AK35	VSS#109	VSS#234	BE95	VSS#359	VSS#484
AK38	VSS#110	VSS#235	BE96	VSS#360	VSS#485
AK41	VSS#111	VSS#236	BE97	VSS#361	VSS#486
AK44	VSS#112	VSS#237	BE98	VSS#362	VSS#487
AK48	VSS#113	VSS#238	BE99	VSS#363	VSS#488
AL2	VSS#114	VSS#239	BE100	VSS#364	VSS#489
AL22	VSS#115	VSS#240	BE101	VSS#365	VSS#490
AL24	VSS#116	VSS#241	BE102	VSS#366	VSS#491
AL27	VSS#117	VSS#242	BE103	VSS#367	VSS#492
AL30	VSS#118	VSS#243	BE104	VSS#368	VSS#493
AL32	VSS#119	VSS#244	BE105	VSS#369	VSS#494
AL35	VSS#120	VSS#245	BE106	VSS#370	VSS#495
AL37	VSS#121	VSS#246	BE107	VSS#371	VSS#496
AL40	VSS#122	VSS#247	BE108	VSS#372	VSS#497
AL42	VSS#123	VSS#248	BE109	VSS#373	VSS#498
AL45	VSS#124	VSS#249	BE110	VSS#374	VSS#499
AL5	VSS#125	VSS#250	BE111	VSS#375	VSS#500

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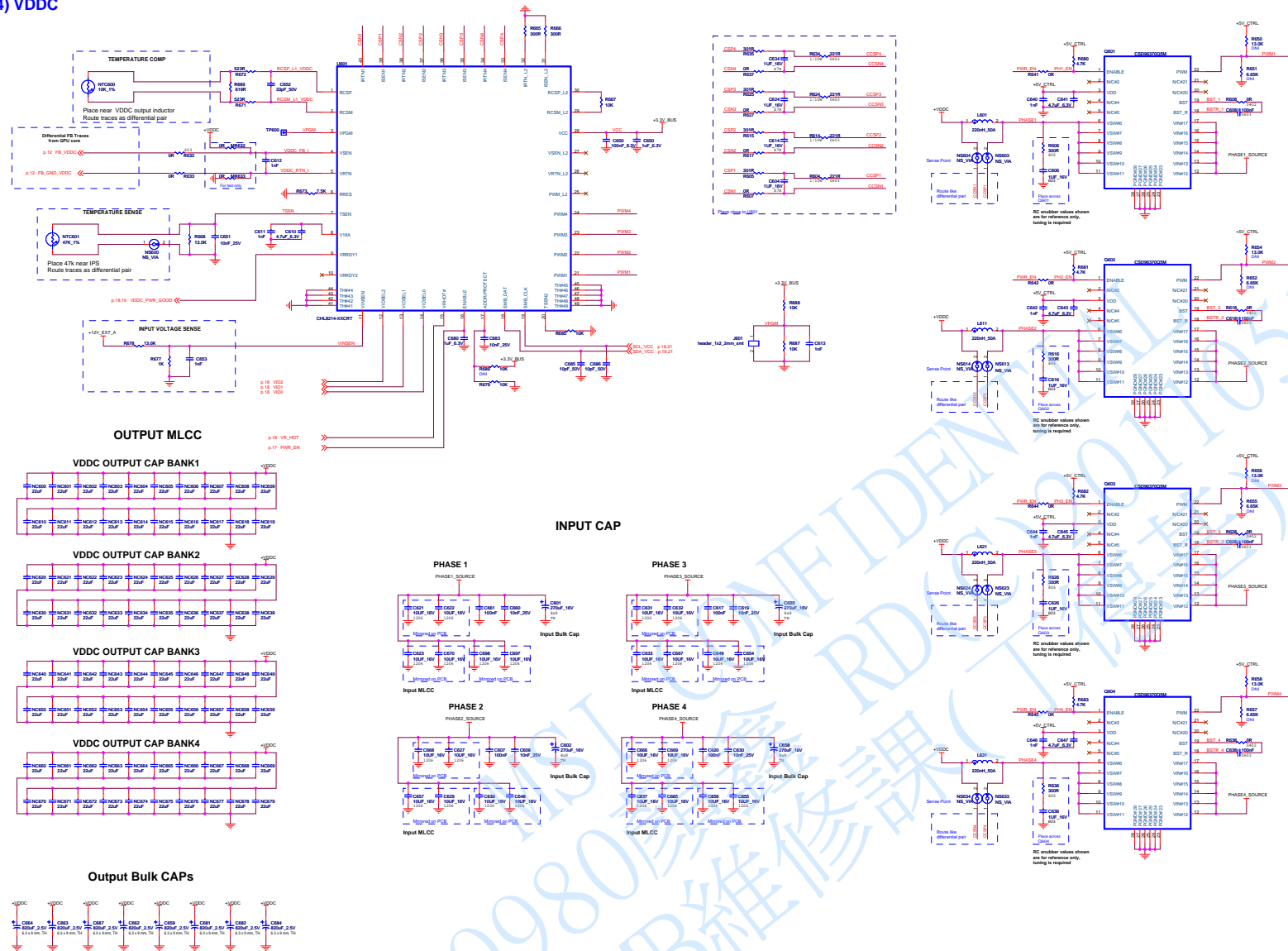
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Sheet 13 of 23
Rev 1

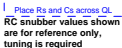
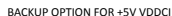
Doc No. 105-C224XX-00A

ASIC GND

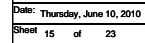
(14) VDDC



(15) VDDCI



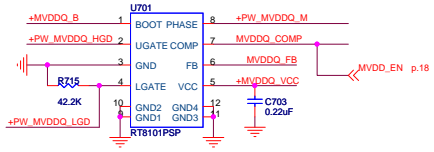
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Title VDDCI

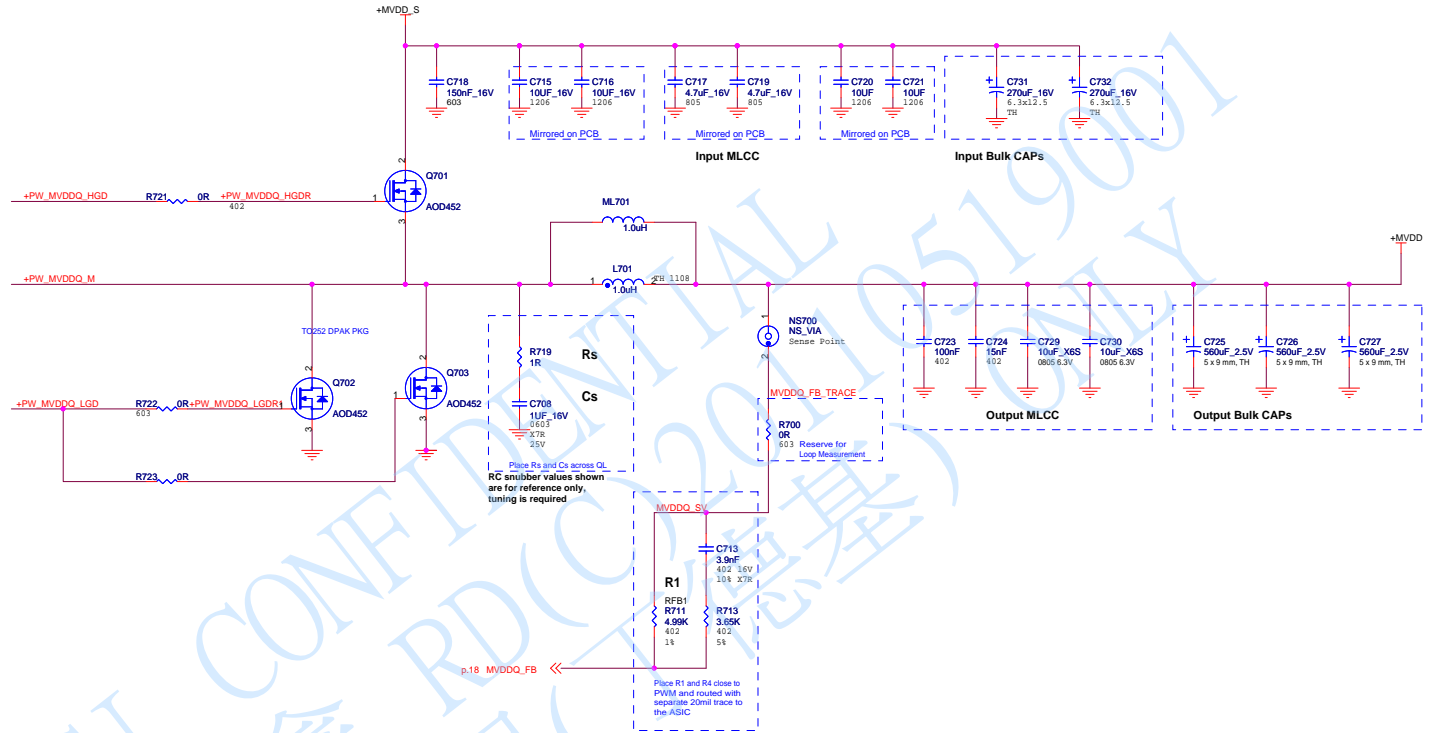


(16) MVDD

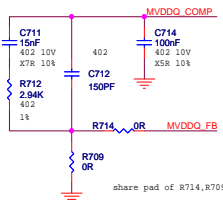


Layout guideline

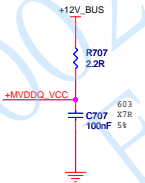
- 1-Position the controller (U703) such that LGate(pin4) is the closest to gate of the MOSFETs. You can place the gate resistors R721 and R722 next to the gate of the MOSFETs. Make the gate drive traces (PW_MVDDQ_LGD and PW_MVDDQ_HGD) as short and as wide as possible to reduce the trace inductance.
- 2-Place the bypass capacitors for Vcc as well as Boost caps as close to the controller as possible. They are as follows:
Vcc bypass cap is C703, and Boost cap is C705.
- 3-Voltage amplifier compensation network. Place C714 close to the pin 7. Place the rest of the compensation network close to the pins 7 and 6. These are R710, R711, R713, C713 and R712, C711 and C712.



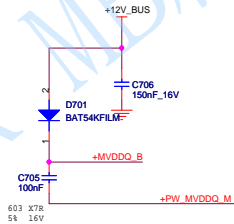
COMPENSATION CIRCUIT



FILTERED SMPS VCC



BOOT CIRCUIT



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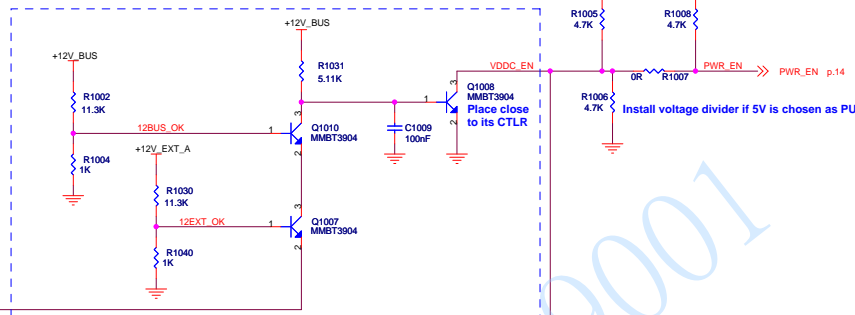
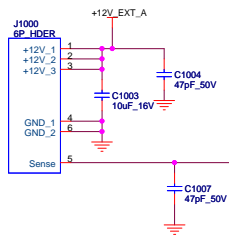
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Sheet 16 of 23

Rev 1

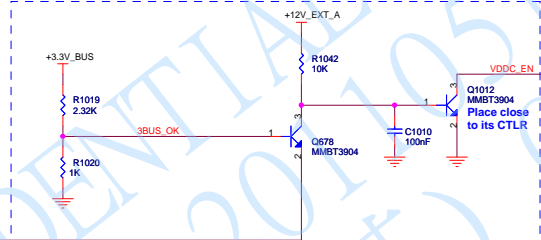
Title MVDD

Doc No. 105-C224XX-00A

(17) Barts POWER MGMNT



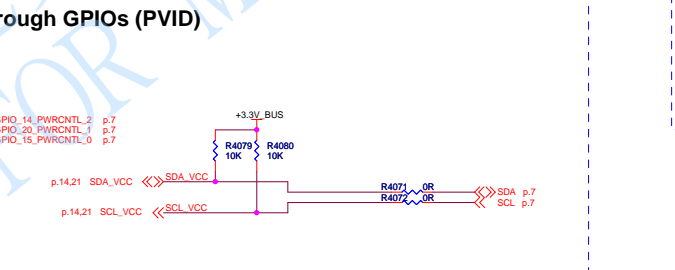
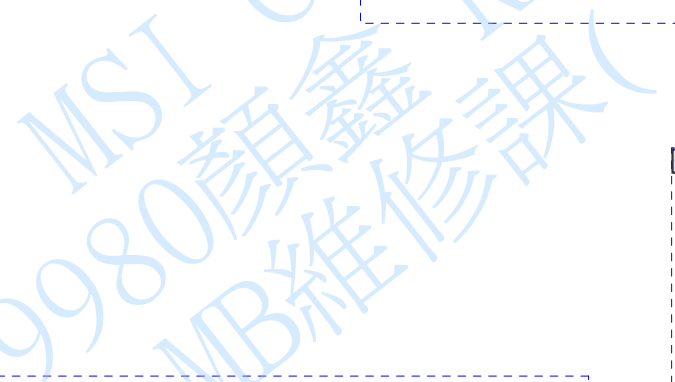
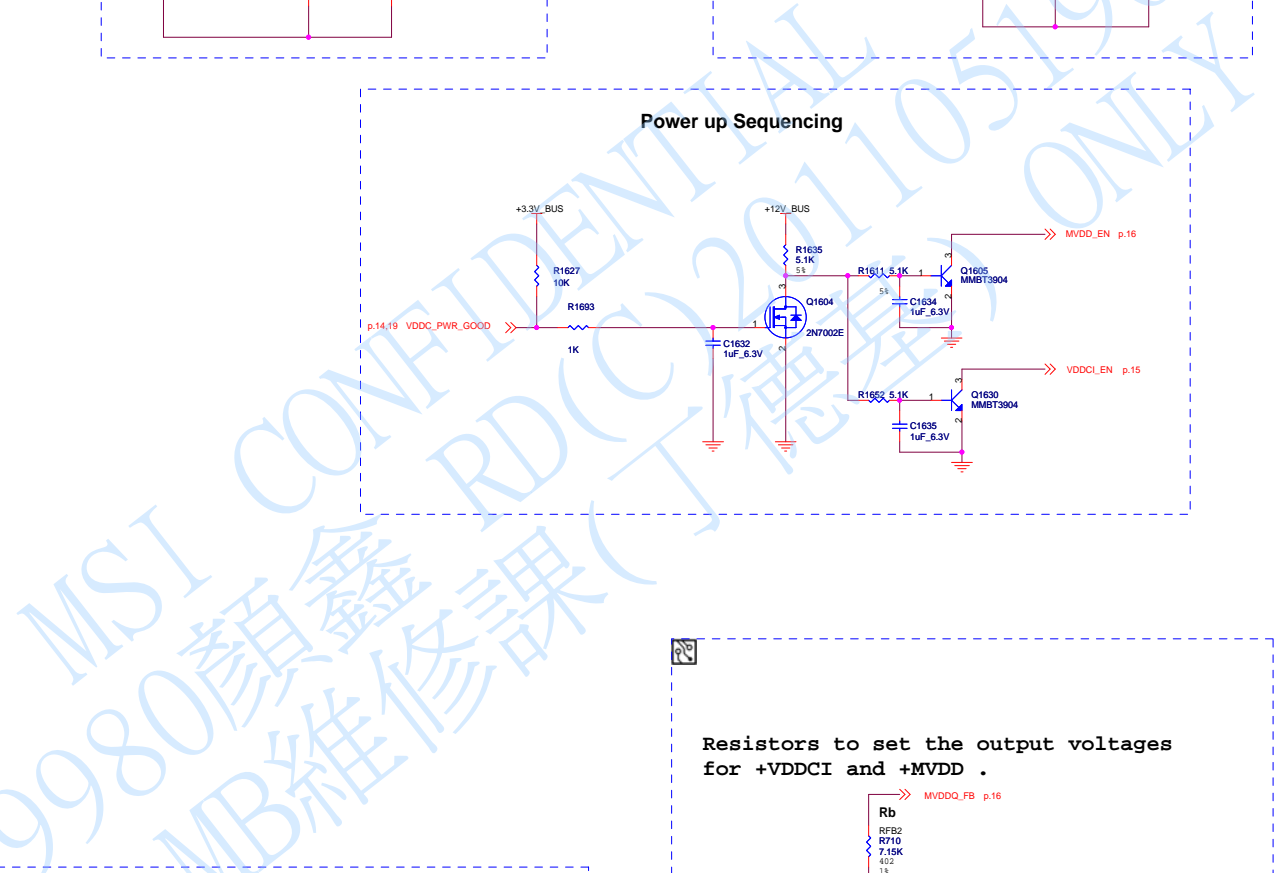
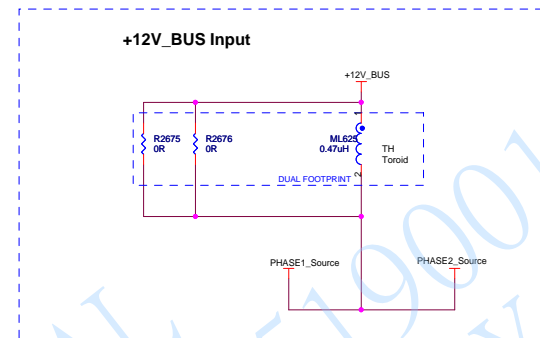
BUS 12V and AUX A Power up Seq



BUS 3.3V Power up Seq



Shutdown for CTF



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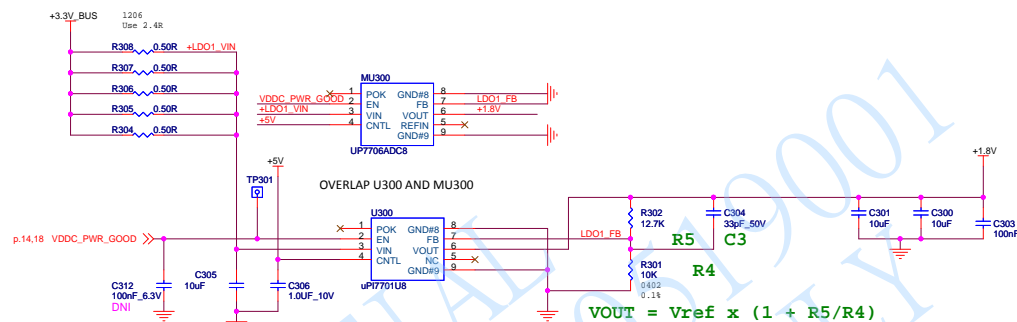
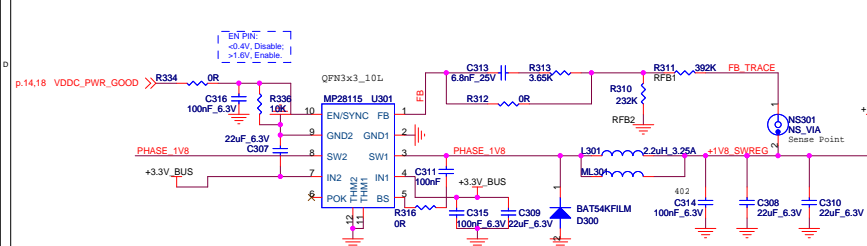
Rev 1

Doc No.	105-C224XX-00A
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(19) Barts Small Rail Regulators

LDO #1: Vin = 2.1V to 3.6V MAX Vout = +1.8V +/- 2% Iout = 2.3A (TBV) RMS MAX

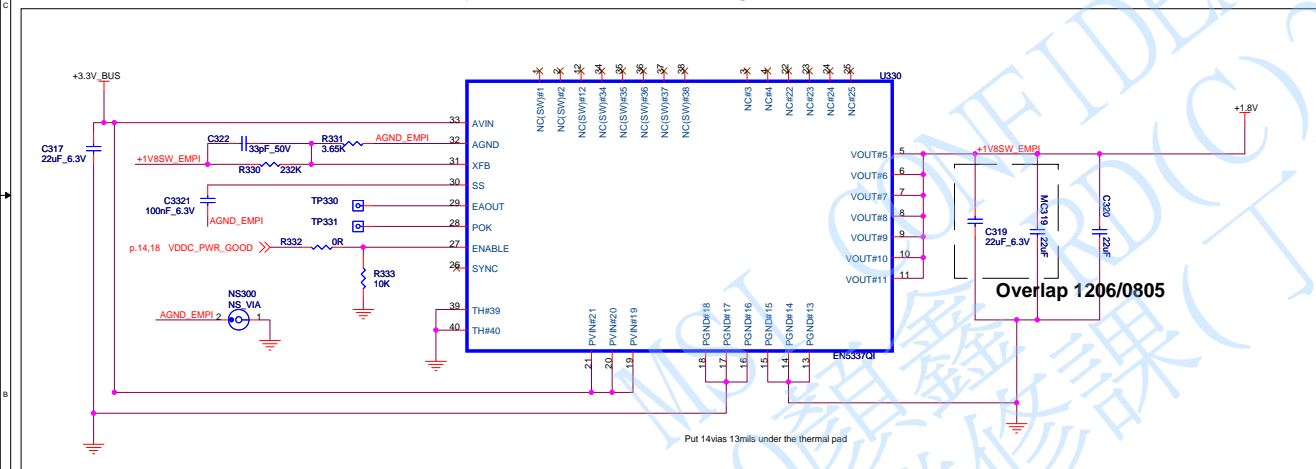
PCB: 50 to 70mm sq. copper area for cooling



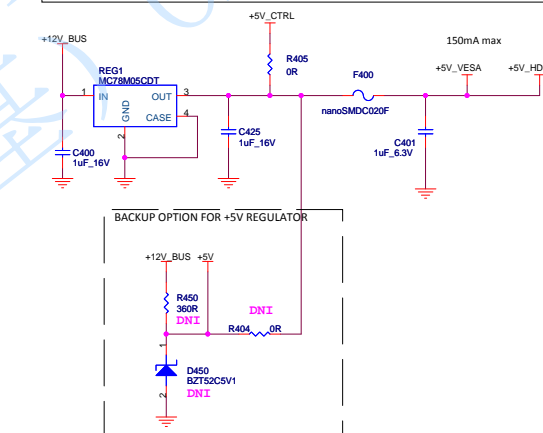
$$V_{OUT} = V_{ref} \times (1 + R_5/R_4)$$

Regulators for +5V, +5V_VESA and +5V_HDMI
Iout max = 150mA (DVI+HDMI)

Other cheaper solution at 5MHz switching for 1.8V



Overlap 1206/0805

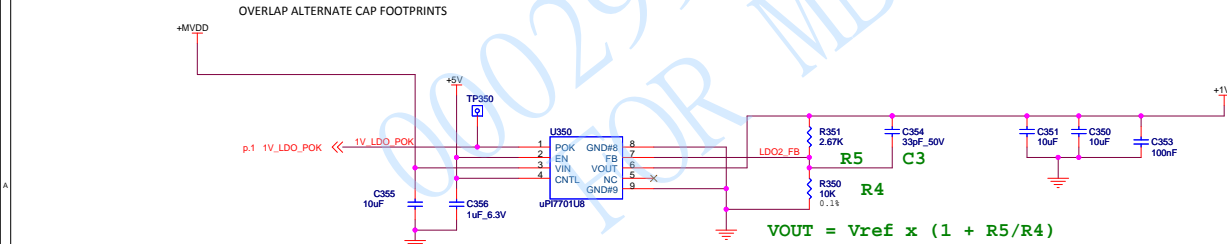
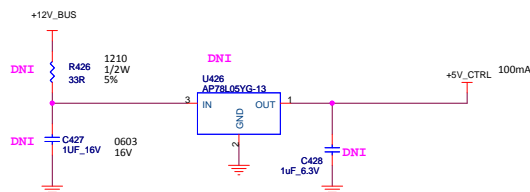


optional 5V power for VDDC regulator;

LDO #2: Vin = +1.35V to 1.8VMAX Vout = +1V +/- 2% Iout = 1.7A (TBV) RMS MAX

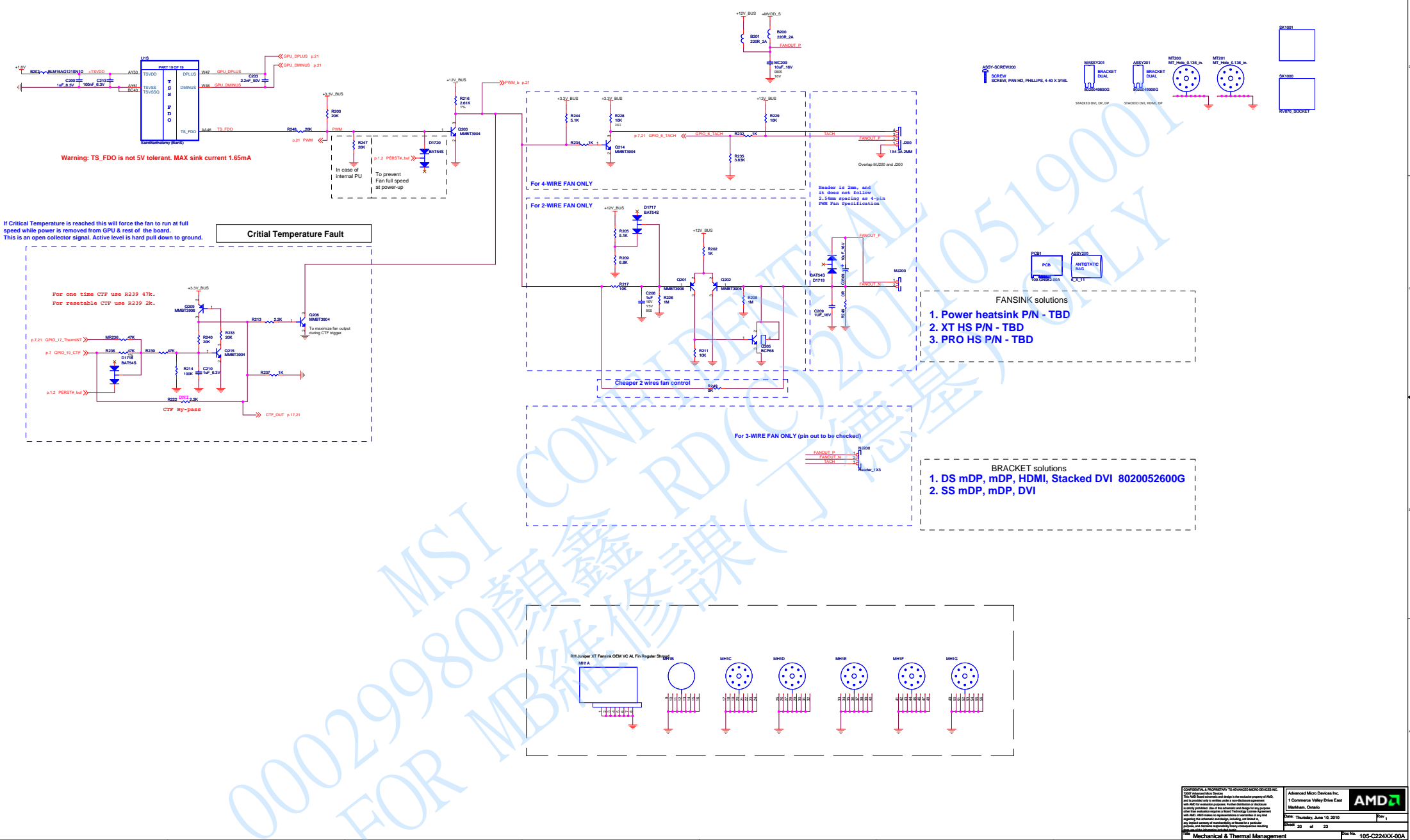
PCB: 50 to 70mm sq. copper area for cooling

OVERLAP ALTERNATE CAP FOOTPRINTS

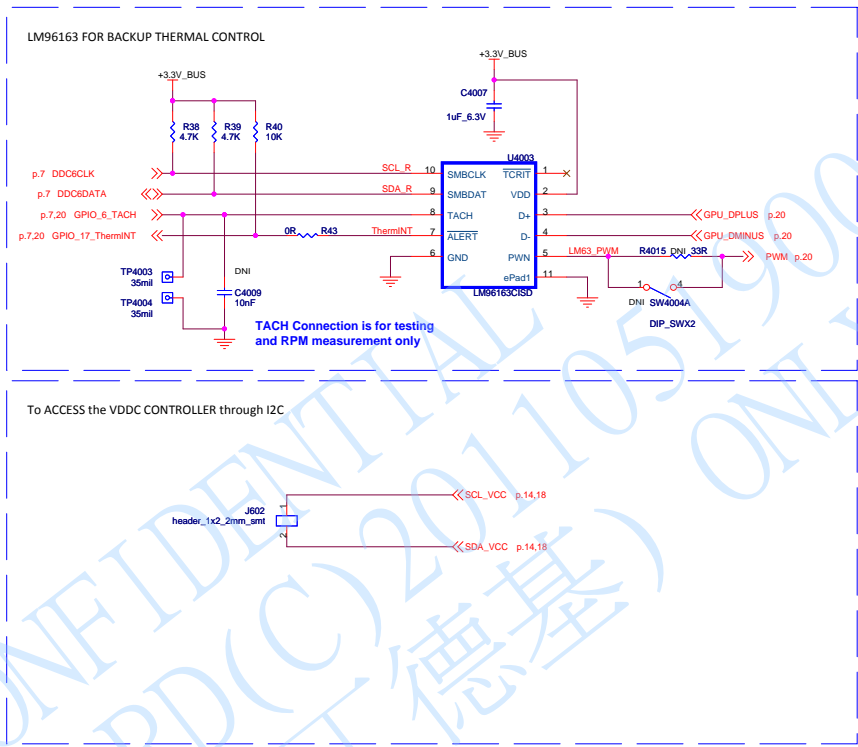
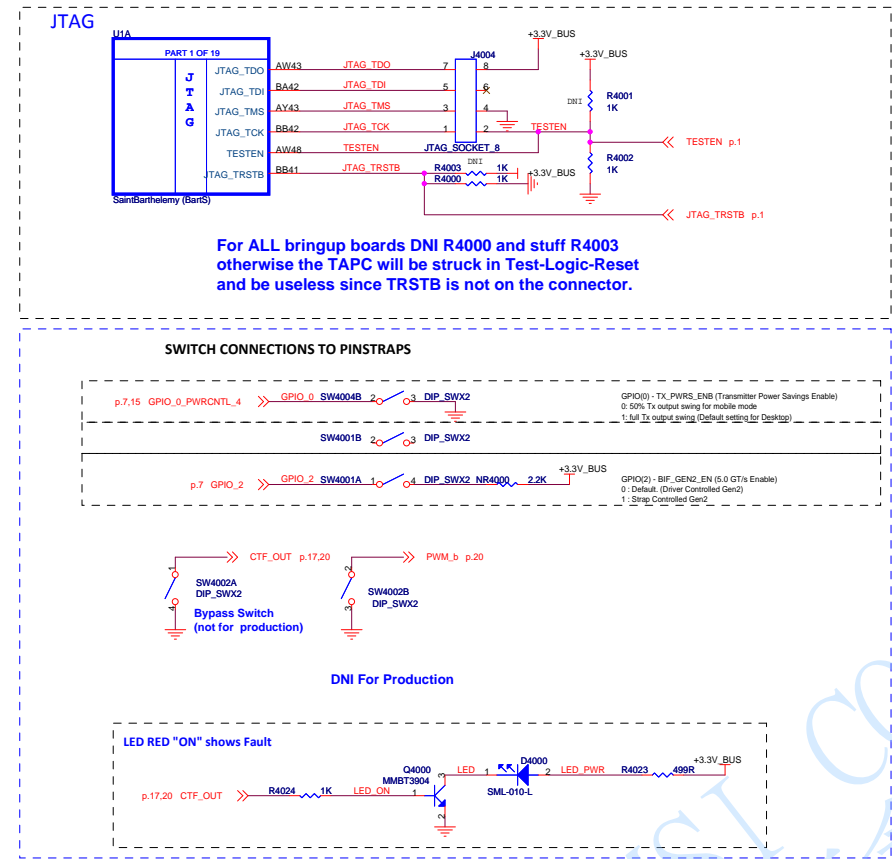


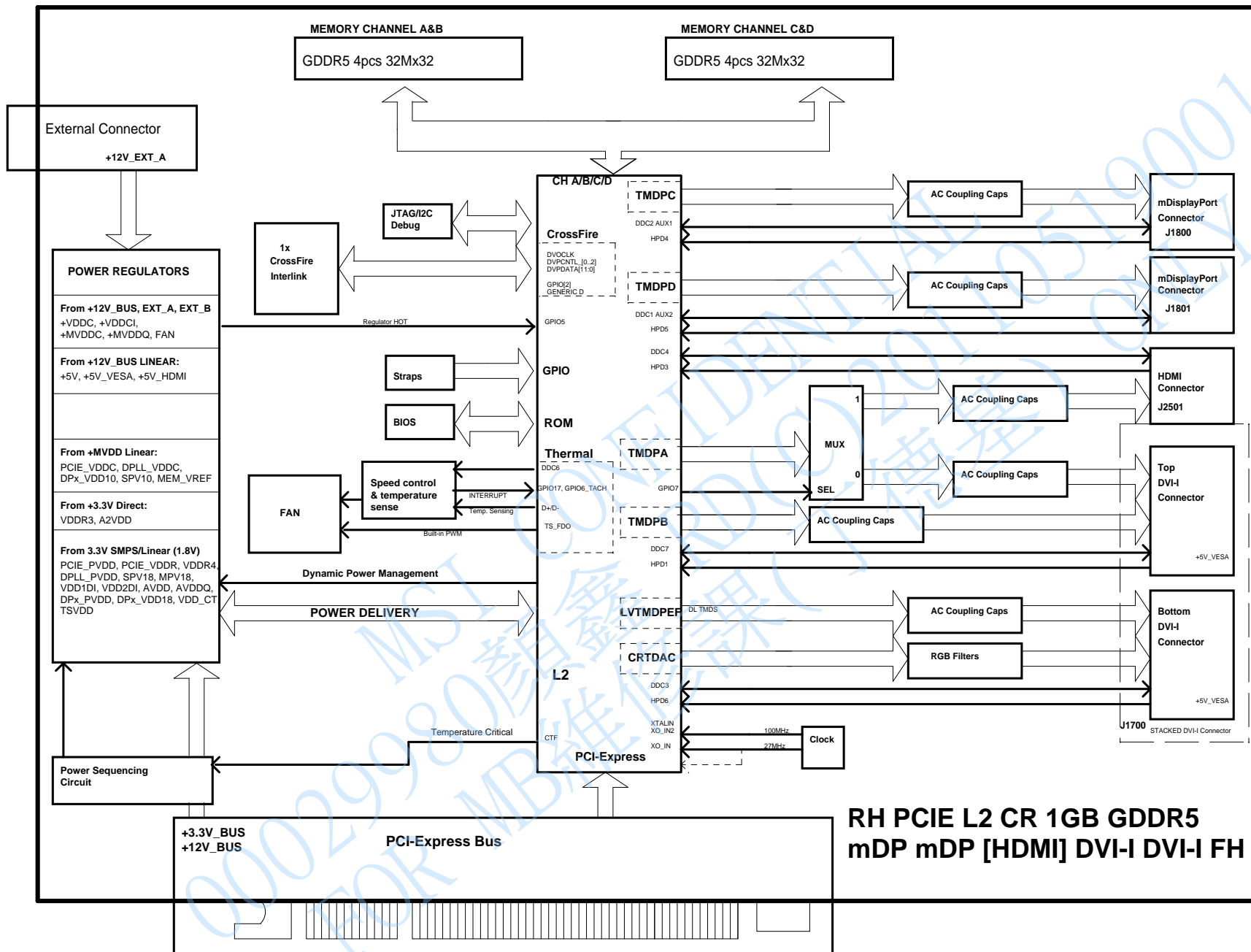
$$V_{OUT} = V_{ref} \times (1 + R_5/R_4)$$

(20) Barts Mechanical and Thermal Management



(21) Barts Debug Circuits





RH PCIE L2 CR 1GB GDDR5
mDP mDP [HDMI] DVI-I DVI-I FH

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Date: Thursday, June 10, 2010 Rev 1
Sheet 22 of 23 Doc No. 105-C224XX-00A





Title	Schematic No.	Date:
RH Barts GDDR5 DP-HDMI-DVII-DVII	105-C224XX-00A	Thursday, June 10, 2010

REVISION HISTORY	NOTE: This schematic represents the PCB, it does not represent any specific SKU. For Stuffing options (component values, DNI , ? please consult the product specific BOM. Please contact AMD representative to obtain latest BOM closest to the application desired.	Rev 1
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Sch Rev	PCB Rev	Date	REVISION DESCRIPTION
0	00A	10/06/2010	Initial release. Based on C220

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